12-20-00

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Tongbi Jiang and Zhiqiang Wu

For: NOVEL ZERO INSERTION FORCE SOCKETS USING NEGATIVE THERMAL EXPANSION MATERIALS

Atty Dkt: 23804-G99999

Serial No: unassigned (second continuation of S.N. 09/248,932)

Filed: Concurrently herewith

Group Art Unit: 2839 (anticipated)

Examiner: Tulsdias C. Patel (anticipated) (703) 308-1736

CERTIFICATE OF EXPRESS MAIL

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I hereby certify that this paper or fee is being deposited with the United States Postal Service "EXPRESS MAIL POST OFFICE TO ADDRESSEE" service under 37 C.F R. 1.10 on the date indicated above and is addressed to: Assistant Commissioner for Patents, Washington, D C 20231.

SIGNATURE: D. Rypacek
D. Rypacek

Assistant Commissioner for Patents
Washington, DC 20231

PRELIMINARY AMENDMENT

Sir:

This paper accompanies a Request for Filing a Second Continuation of the above-referenced application ("the '932 application"), and is accompanied by a check for the appropriate filing fees as calculated in that Request. If any payments associated with this or any of the accompanying papers are incorrect in amount, the Commissioner is hereby authorized to charge any fees or credit any overpayents to Winstead Sechrest & Minick Deposit Account No. 23-2426/23804-P002C2.

Prior to examination on the merits, please amend the application as follows:

Please cancel claims 1-17.

Please add the following new claims:

18. (new) A method of forming a socket for receiving a terminal pin from an electronic component therein, comprising:

forming a layer of a first material on an upper surface of a substrate;

forming a layer of a second material on said said layer of first material; and

forming an aperture in said first and second layers to expose said upper surface of said substrate;

wherein said first material has a positive coefficient of thermal expansion and said second material has a negative coefficient of thermal expansion.

19. (new) A method in accordance with claim 18, further comprising:

forming an electrical contact pad on said substrate such that said contact pad is at least partially exposed within said aperture.

20. (new) A method in accordance with claim 18, wherein said first material is a material selected from the group: silicon oxide, silicon dioxide, silicon nitride, and Si_3N_4.

21. (new) A method in accordance with claim 18, wherein said first material is a polyimide.

22. (new) A method in accordance with claim 18, wherein said second material is zirconium tungstate.

23. (new) A method in accordance with claim 22, wherein said zirconium tungstate is single-crystal zirconium tungstate.

24. (new) A method in accordance with claim 22, wherein said zirconium tungstate is amorphous zirconium tungstate.

25. (new) A method in accordance with claim 22, wherein said zirconium tungstate is polymer bound zirconium tungstate.

26. (new) A method in accordance with claim 18, further comprising:

applying an interfacial material between said layer of first material and said layer of second material to permit relative movement between said layer of first material and said layer of second material.

27. (new) A method in accordance with claim 18, wherein said substrate is ceramic.

28. (new) A method in accordance with claim 18, wherein said substrate is a package of an integrated circuit.

29. (new) A method in accordance with claim 18, wherein said layer of first material is bonded to said substrate using a spin-on and photo define/etch process.

30. (new) A method in accordance with claim 18, wherein said step of forming said aperture comprises forming a first aperture in said layer of first material and a second aperture in said layer of second material, wherein said second aperture has a linear dimension smaller than said first aperture.

31. (new) A method of electrically connecting an electronic component having a contact pin

extending therefrom to a contact pad on a substrate, comprising:

forming a layer of a first material on an upper surface of said substrate;

forming a layer of a second material on said said layer of first material; and

forming an aperture in said first and second layers to expose said upper surface of said substrate;

wherein said first material has a positive coefficient of thermal expansion and said second material has a negative coefficient of thermal expansion;

and wherein said method further comprises:

heating said layer of first material and said layer of second material to a temperature substantially above a range of normal operating temperatures for said electronic component;

inserting said contact pin into said aperture; and

cooling said layer of first material and said layer of second material to a temperature within said range of normal operating temperatures for said electronic component.

32. (new) A method in accordance with claim 31, further comprising:

forming an electrical contact pad on said substrate such that said contact pad is at least partially exposed within said aperture.

33. (new) A method in accordance with claim 31, wherein said first material is a material selected from the group: silicon oxide, silicon dioxide, silicon nitride, and Si_3N_4.

34. (new) A method in accordance with claim 31, wherein said first material is a polyimide.

35. (new) A method in accordance with claim 31, wherein said second material is zirconium tungstate.

36. (new) A method in accordance with claim 35, wherein said zirconium tungstate is single-crystal zirconium tungstate.

37. (new) A method in accordance with claim 35, wherein said zirconium tungstate is amorphous zirconium tungstate.

38. (new) A method in accordance with claim 35, wherein said zirconium tungstate is polymer bound zirconium tungstate.

39. (new) A method in accordance with claim 31, further comprising:

applying an interfacial material between said layer of first material and said layer of second material to permit relative movement between said layer of first material and said layer of second material.

40. (new) A method in accordance with claim 31, wherein said substrate is ceramic.

41. (new) A method in accordance with claim 31, wherein said substrate is a package of an integrated circuit.

42. (new) A method in accordance with claim 31, wherein said layer of first material is bonded to said substrate using a spin-on and photo define/etch process.

43. (new) A method in accordance with claim 31, wherein said step of forming said aperture comprises forming a first aperture in said layer of first material and a second aperture in said layer of second material, wherein said second aperture has a linear dimension smaller than said first aperture.

44. (new) A method in accordance with claim 31, wherein said step of heating said layer of first material and said layer of second material comprises heating said layer of first material and said layer of second material to a temperature of between approximately 200°C and 250°C.

45. (new) A method in accordance with claim 44, wherein a normal operating temperature for said electronic component is approximately 100°C.

46. A method in accordance with claim 31, wherein said step of cooling said layer of first material and said layer of second material comprises cooling said layer of first material at a rate slower than the rate at which said layer of second material is cooled.

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No new matter has been added by way of these amendments. It is believed that the application is in proper form and condition for allowance. Examination and allowance of the claims is hereby requested. If the Examiner believes that the application can be placed in even better condition for allowance, he or she is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,

Date: 19-DEC-2000

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